



Caliber Interconnect Solutions

Design for perfection

SI Failure Analysis Report



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INPUTS

- Layout (.brd) file
- Stackup



STACKUP

Color	Name	Type	Thickness (mils)	Material	Conductivity (S/m)	Dielectric Fill	Dielectric constant	Loss tangent	Translucency	Elevation (mils)
	UNNAMED_1	DIELECTRIC	1	solder_mask	0		3.6	0.02		60.6
■	TOP	METAL	1.8	CDS_COPPER	5.959E+07	roger	3.54	0.004	65	58.8
	UNNAMED_3	DIELECTRIC	4	roger	0		3.54	0.004		54.8
■	GND	METAL	1.2	CDS_COPPER	5.959E+07	fr4	3.8	0.02	65	53.6
	UNNAMED_5	DIELECTRIC	44	fr4	0		3.8	0.02		9.6
■	PWR	METAL	1.2	CDS_COPPER	5.959E+07	fr4	3.8	0.02	65	8.4
	UNNAMED_7	DIELECTRIC	5.6	fr4	0		3.8	0.02		2.8
■	BOTTOM	METAL	1.8	CDS_COPPER	5.959E+07	fr4	3.8	0.02	65	1
	UNNAMED_9	DIELECTRIC	1	solder_mask	0		3.6	0.02		0

Above Stack-up is based on following criterion:

1. Dielectric Material
 - Roger (DK-3.54,DF-0.004)
 - FR4 (DK-3.8, DF-0.02)
2. Solder mask
 - 1 mil thickness
 - DK – 3.6 and DF – 0.002
3. Total board thickness : 61.6mils

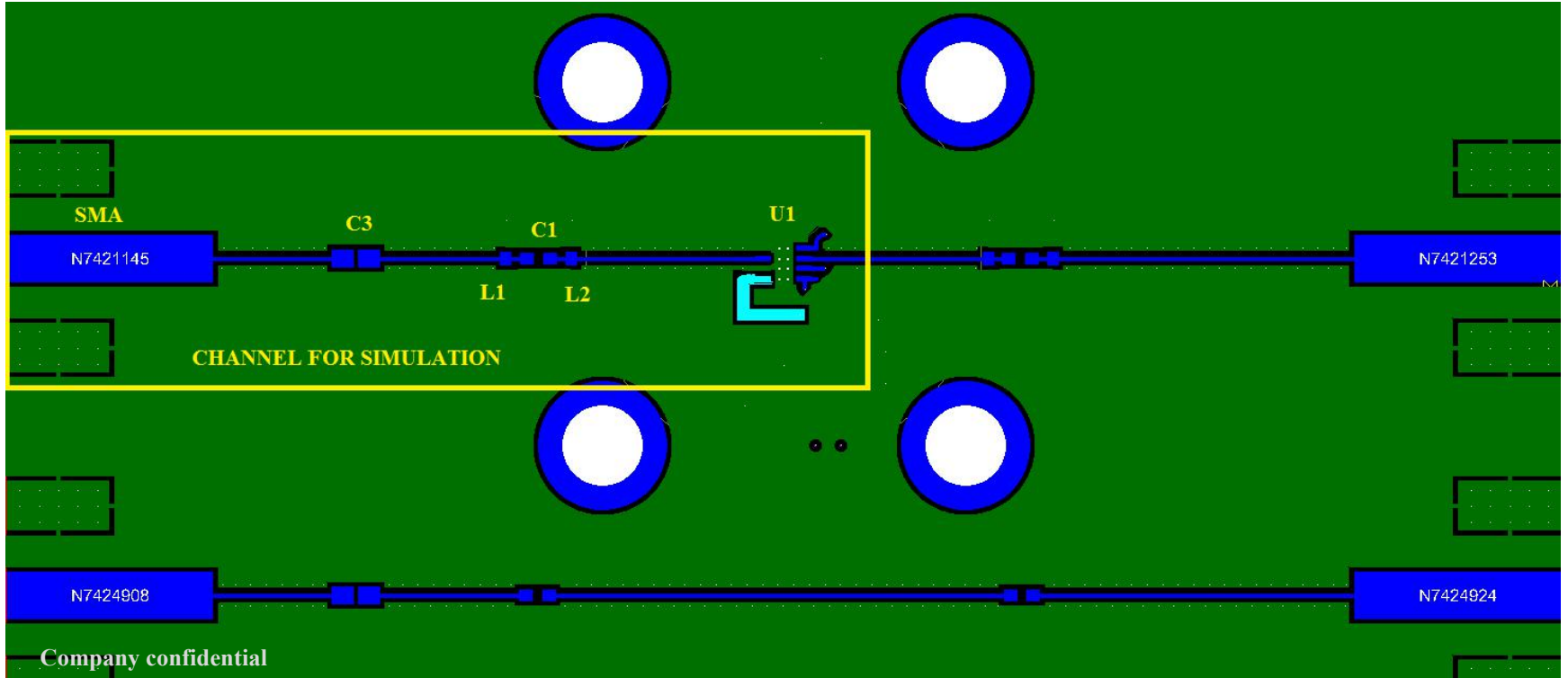


SCOPE OF WORK

Customer Request : In a Assembled board, the impedance-controlled channels are not working at high frequency. DC wise they are fine, not shorted or anything. Simulate the original board condition. Find the root cause of the issue and give suggestion, so that the issue is resolved in the Revised edition.



CHANNEL FOR ANALYSIS





SIMULATION SETUP

Trace Impedance used:

Trace width – 8mil

Ground strip separation – 11mil

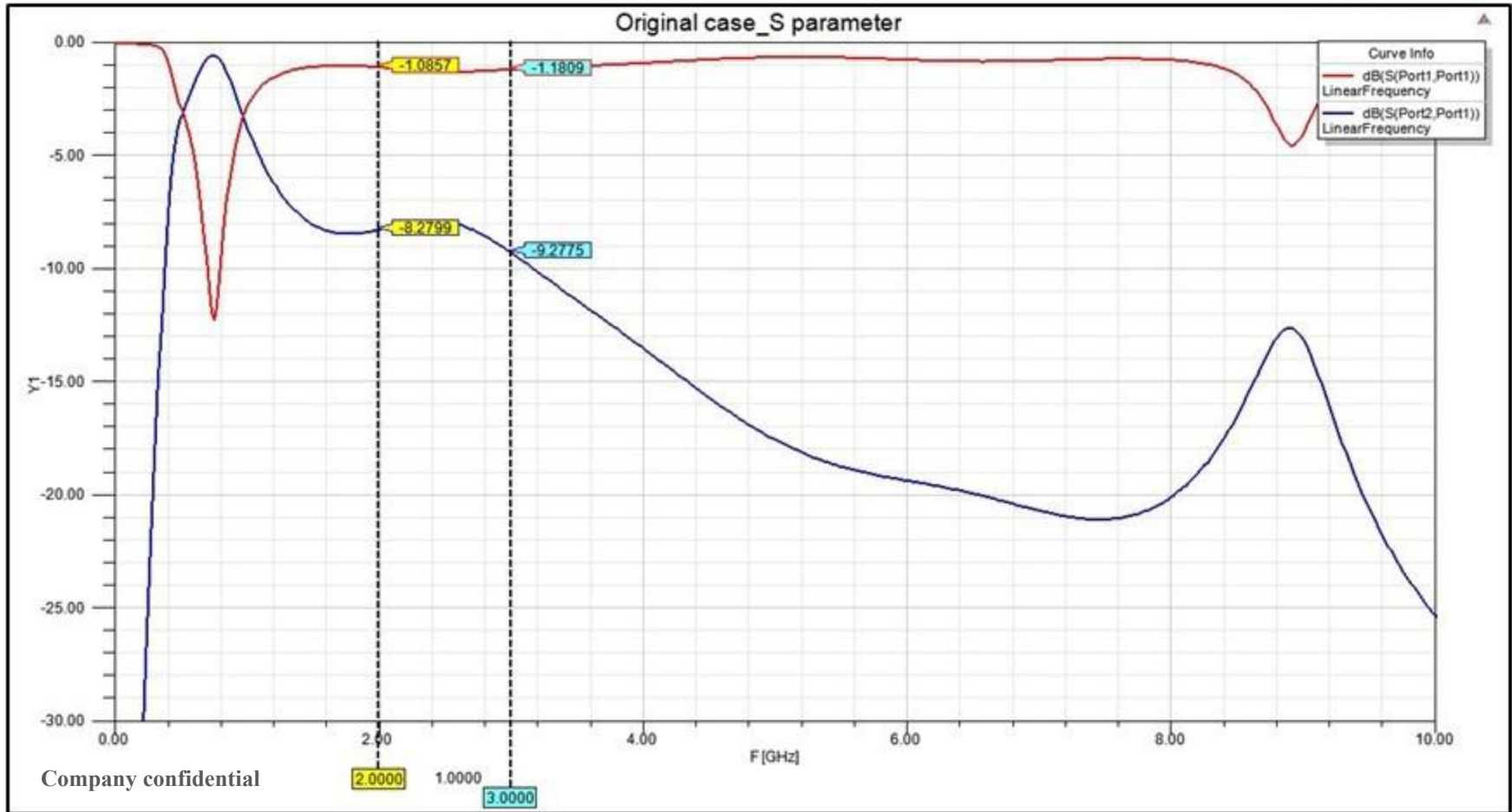
Surface Coplanar Waveguide With Ground 1B

www.polarinstruments.com
Company confidential

Substrate 1 Height	H1	<input type="text" value="4.0000"/>	+/-	<input type="text" value="0.0000"/>	<input type="text" value="4.0000"/>	<input type="text" value="4.0000"/>	<input type="button" value="Calculate"/>
Substrate 1 Dielectric	Er1	<input type="text" value="3.5400"/>	+/-	<input type="text" value="0.0000"/>	<input type="text" value="3.5400"/>	<input type="text" value="3.5400"/>	<input type="button" value="Calculate"/>
Lower Trace Width	W1	<input type="text" value="8.0000"/>	+/-	<input type="text" value="0.0000"/>	<input type="text" value="8.0000"/>	<input type="text" value="8.0000"/>	<input type="button" value="Calculate"/>
Upper Trace Width	W2	<input type="text" value="7.0000"/>	+/-	<input type="text" value="0.0000"/>	<input type="text" value="7.0000"/>	<input type="text" value="7.0000"/>	<input type="button" value="Calculate"/>
Ground Strip Separation	D1	<input type="text" value="11.0000"/>	+/-	<input type="text" value="0.0000"/>	<input type="text" value="11.0000"/>	<input type="text" value="11.0000"/>	<input type="button" value="Calculate"/>
Trace Thickness	T1	<input type="text" value="1.8000"/>	+/-	<input type="text" value="0.0000"/>	<input type="text" value="1.8000"/>	<input type="text" value="1.8000"/>	<input type="button" value="Calculate"/>
Impedance	Zo	<input type="text" value="49.26"/>			<input type="text" value="49.26"/>	<input type="text" value="49.26"/>	<input type="button" value="Calculate"/>
							<input type="button" value="More..."/>



S-Parameter of entire channel – Original board condition



BLUE– Insertion loss

RED – Return loss

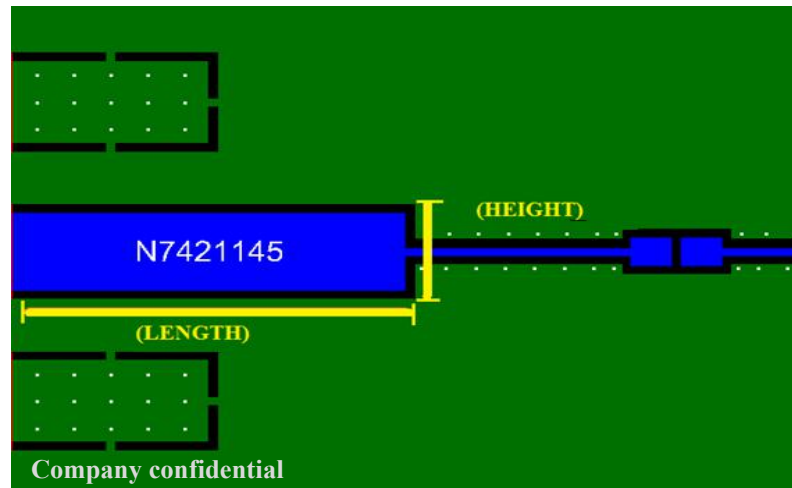


SIMULATION SETUP

We suspect the reason for the failure is due to the SMA pad. It may cause impedance mismatch and hence reflection issues. So we try to optimize the SMA pad for improved performance.

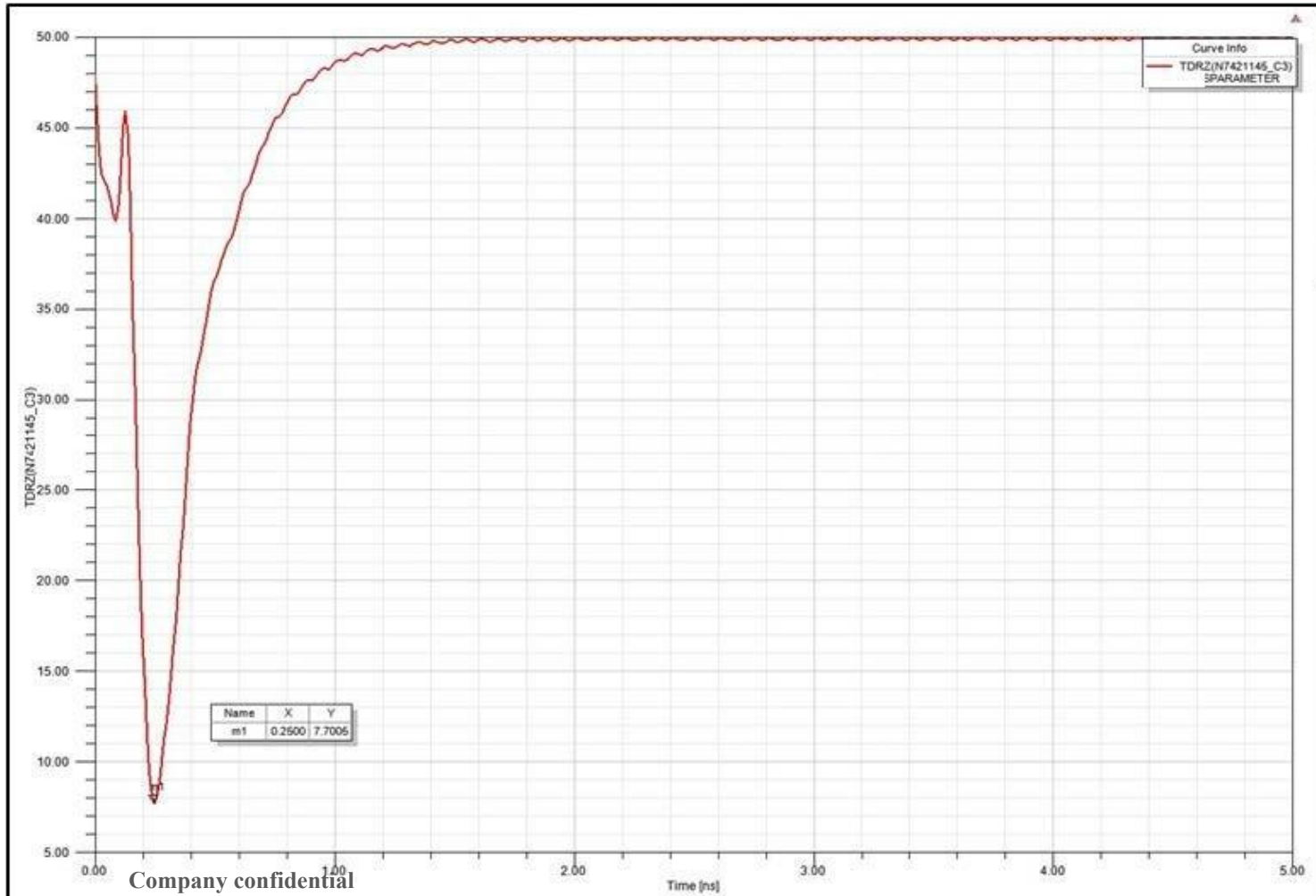
TDR for various dimension of the SMA pad:

- For TDR analysis we considered the trace from component to SMA pad alone.
- The SMA pad length was fixed at 187mil. The height was varied from 20mil to 90mil in steps of 10mil.
- The TDR impedance was simulated for 2 cases; with and without GND clearance.





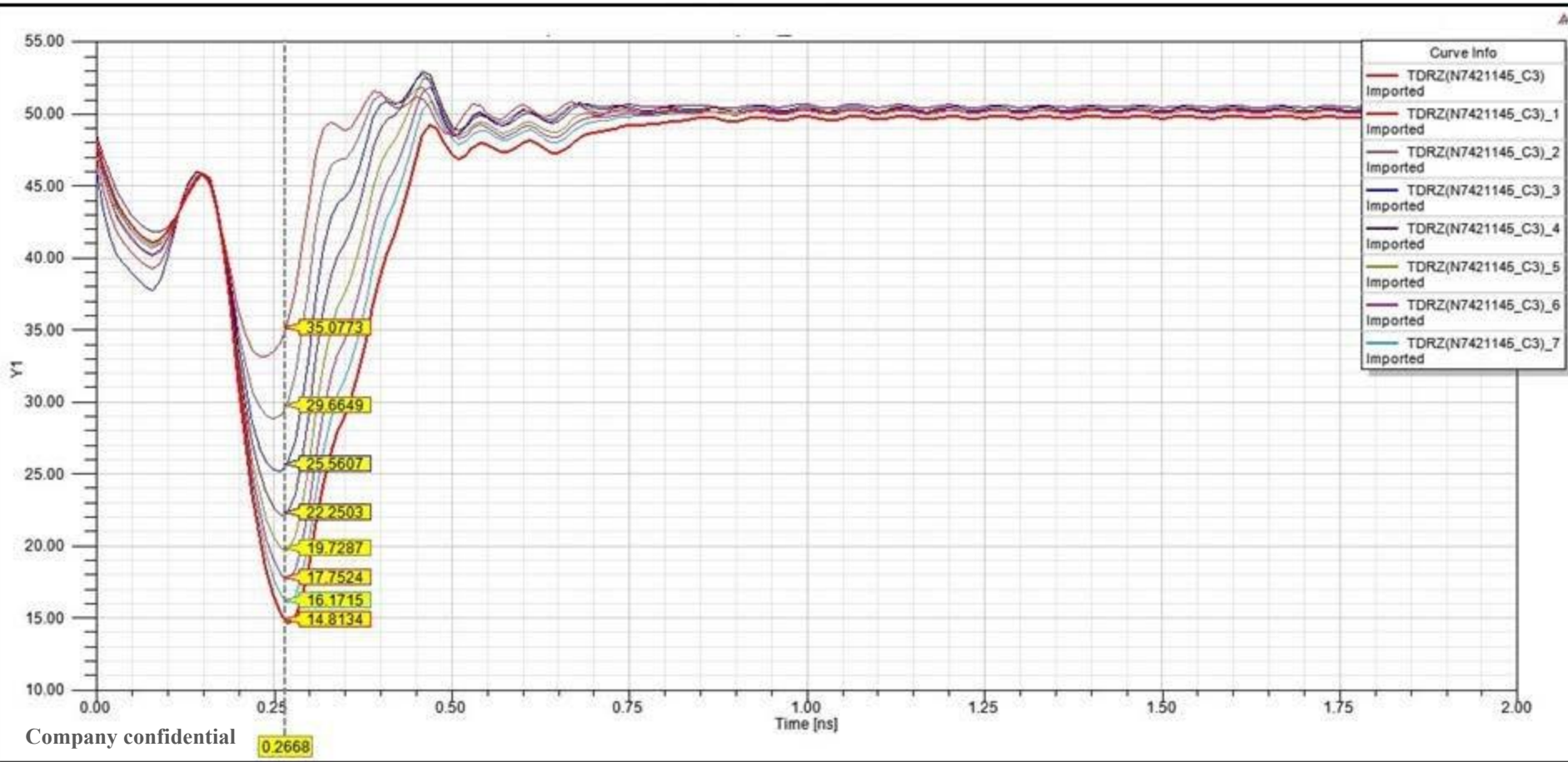
TDR at the SMA pad for original condition



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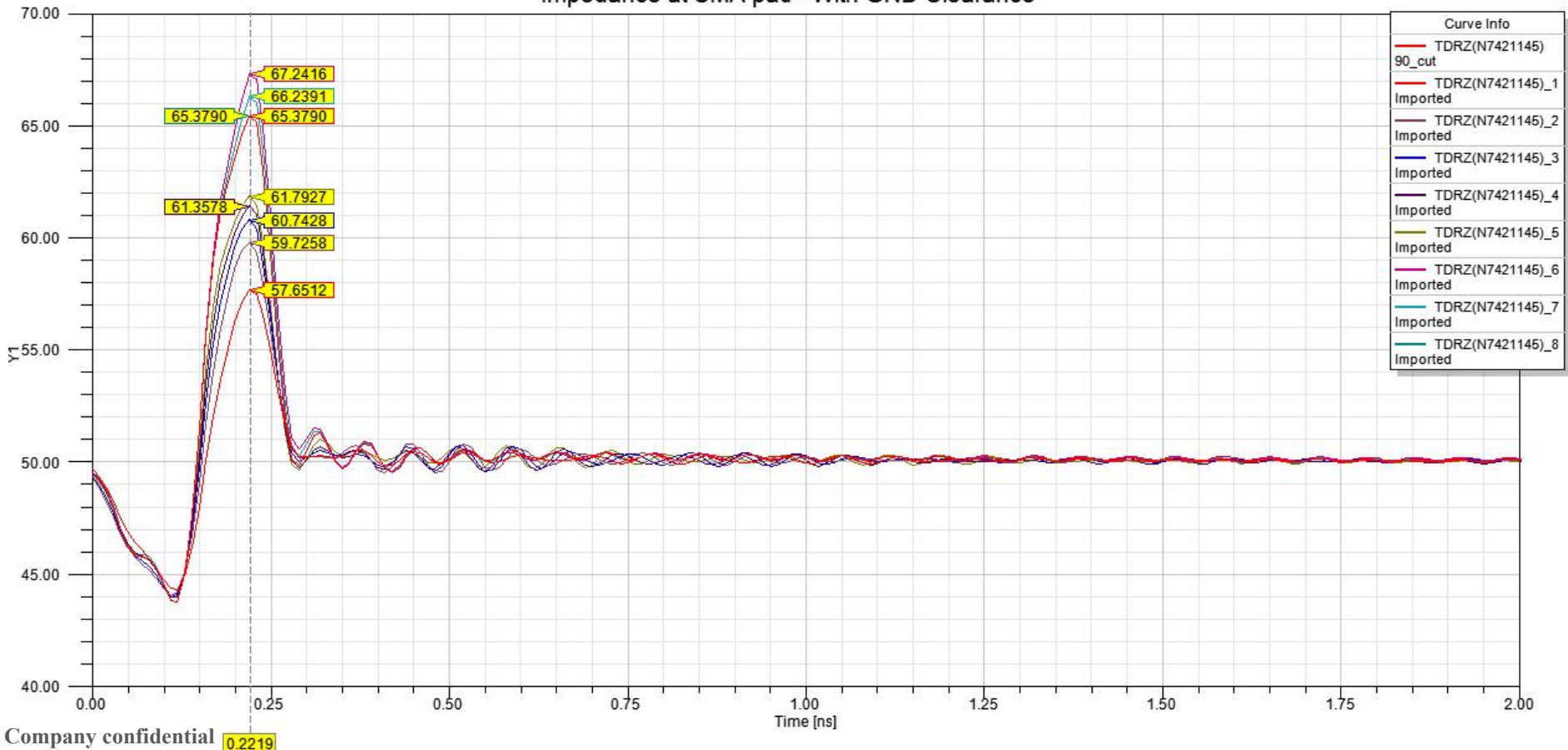
TDR at the SMA pad without GND clearance





TDR at the SMA pad with GND clearance

Impedance at SMA pad - With GND Clearance





TDR impedance at SMA pad

- The table below, summarizes the TDR impedance value at the SMA pad.
- The original SMA pad with dimension 400x90 is around 8ohm.
- The condition of smaller pad height with GND clearance provides relatively better results.

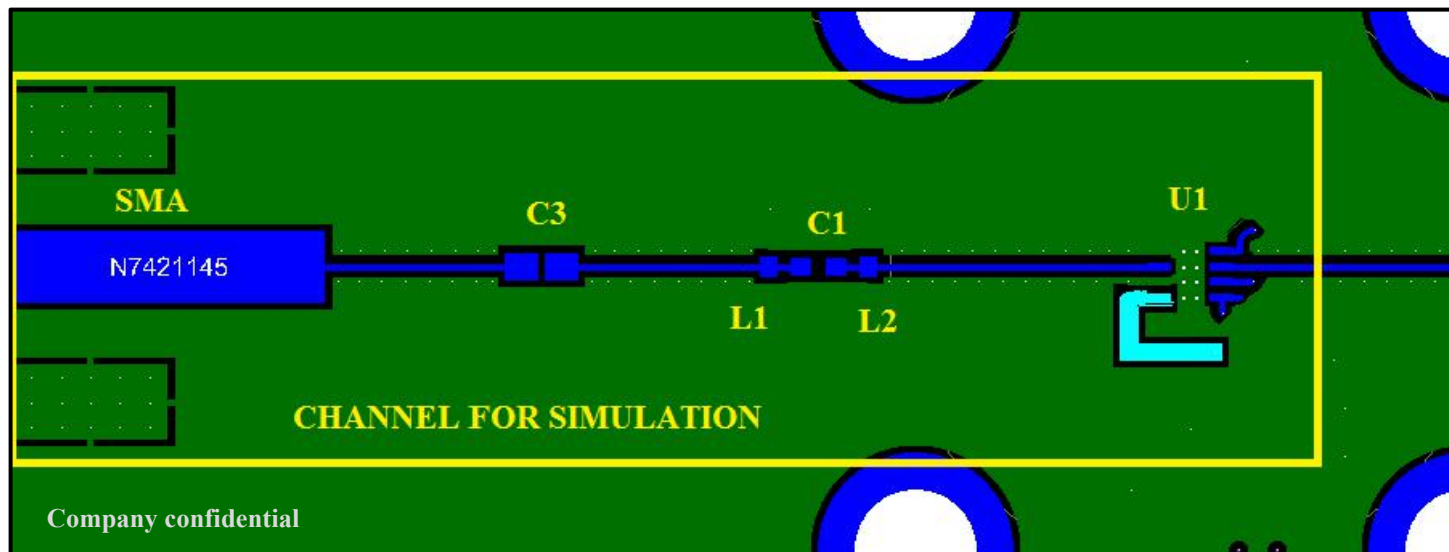
Original SMA Pad (400 x90)		7.7005ohm		
S.NO	LENGTH (mils)	HEIGHT (mils)	IMPEDANCE AT SMApad(OHM)	
			Without GND Clearance	With GND clearance
CASE1	187	20	33.1379	57.67
CASE2	187	30	28.7928	59.81
CASE3	187	40	25.166	60.82
CASE4	187	50	22.0909	61.43
CASE5	187	60	19.7134	61.86
CASE6	187	70	17.6609	67.11
CASE7	187	80	16.0155	66.06
CASE8	187	90	14.6026	65.43



SIMULATION SETUP

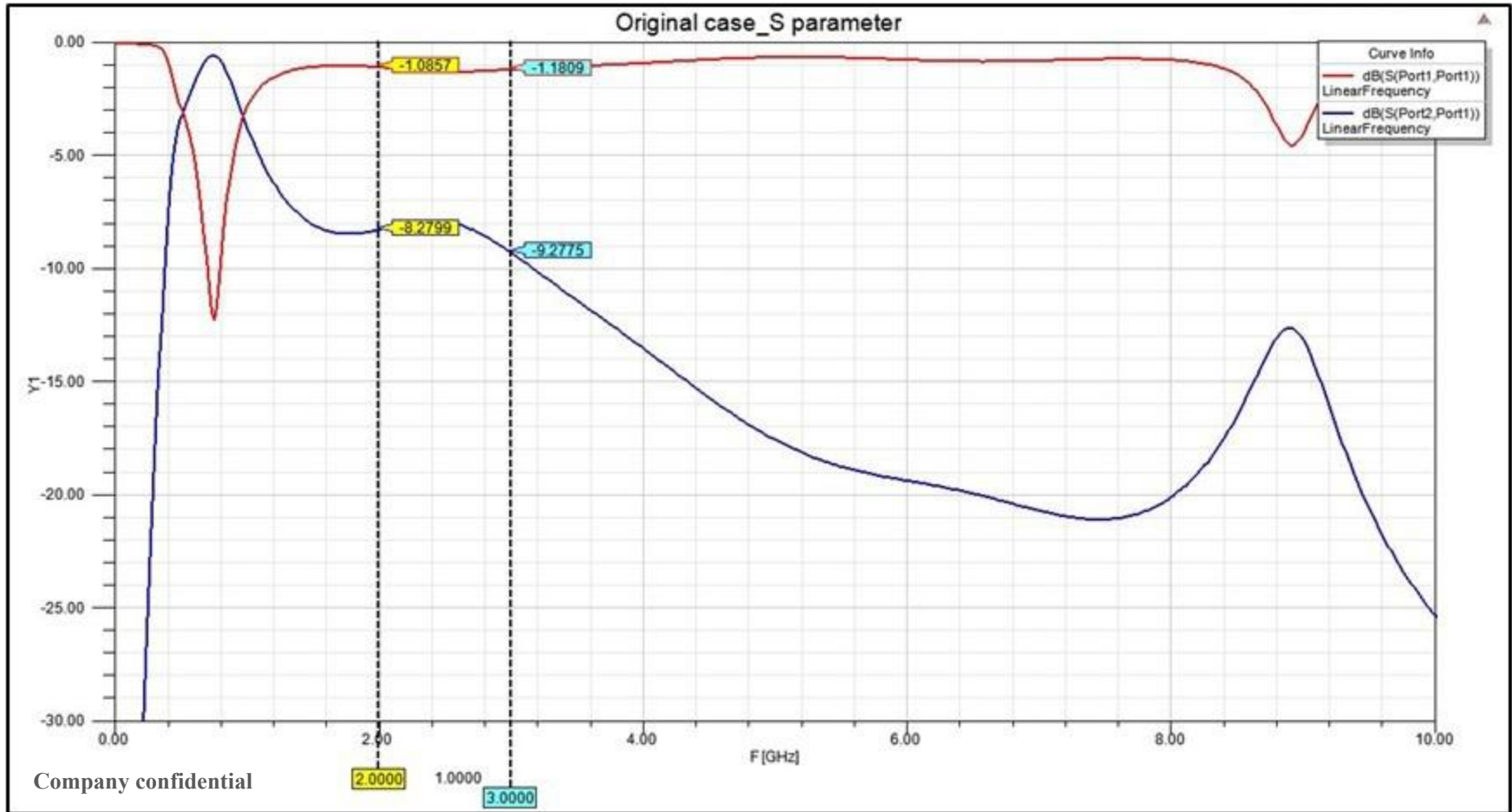
S-Parameter analysis:

- The S-Parameter loss for the entire channel from the U1 to the SMA pad is swept for 10GHz.
- The TDR best case of 187x20mil was alone simulated for S-Parameter.
- GND clearance (exact size of pad) for all the component pad was provided in the “GND” layer.





S-Parameter of entire channel – Original board condition

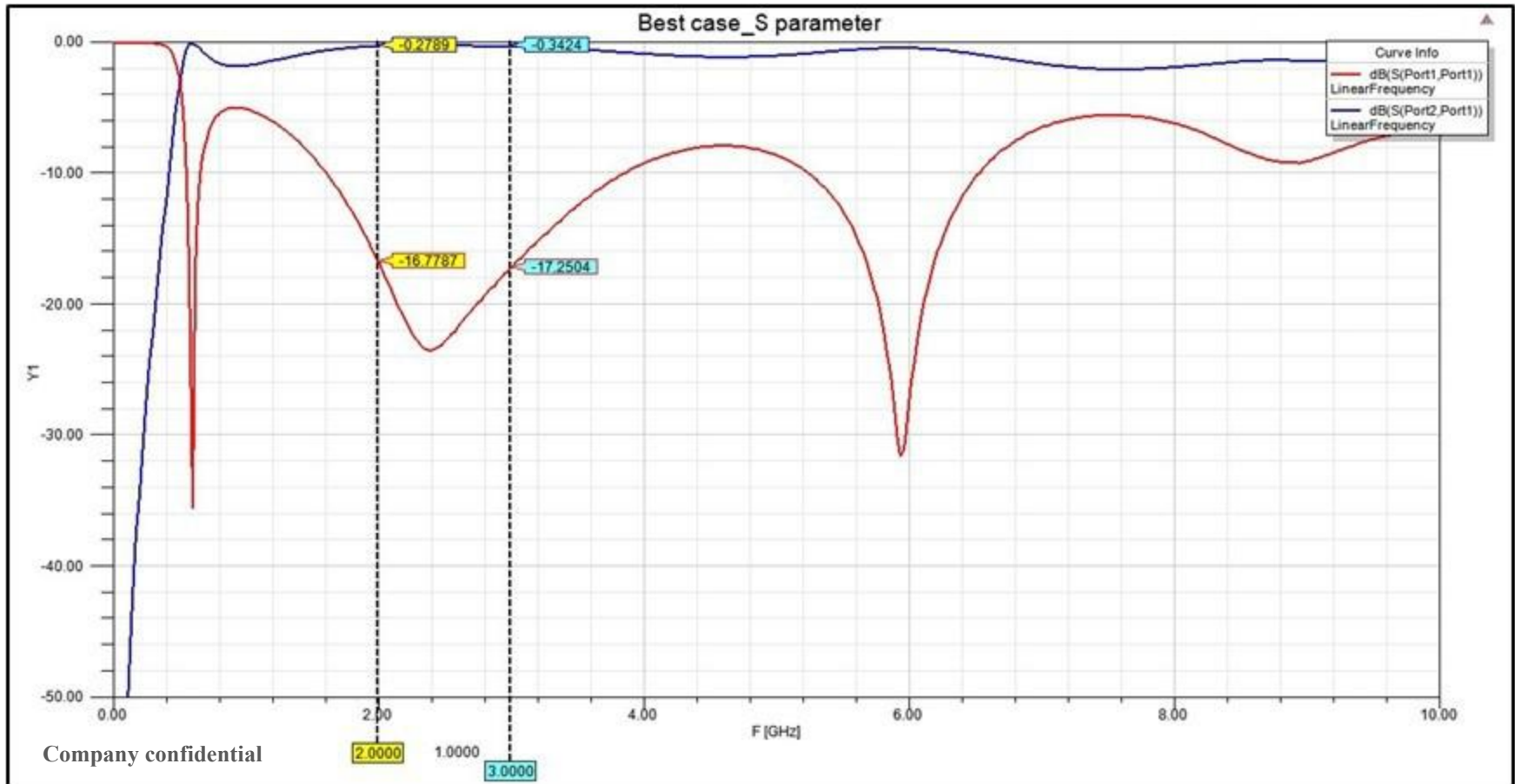


BLUE– Insertion loss

RED – Return loss



S-Parameter of entire channel – Best case



BLUE– Insertion loss

RED – Return loss



S-Parameter result

- The table below, summarizes the S-Parameter result for best and original board condition

CASES	INSERTION LOSS (db)		RETURN LOSS (db)	
	@ 2 GHz	@ 3 GHz	@ 2 GHz	@ 3 GHz
ORIGINALBOARD CONDITION	-8.2799	-9.2775	-1.0857	-1.1809
BEST CASE	-0.2789	-0.3424	-16.7787	-17.2504



RESULT SUMMARY

- The TDR and S-Parameter simulation were carried out using ANSYS Siwave and ANSYS Designer tools.
- The modification done to improve the result are:
 1. Change SMA pad size to 187x20mils
 2. GND clearance in 1 layer “GND” for all the component pads
 3. Trace width used 8mil with 11mil clearance.



CUSTOMER FEEDBACK

Customer Feedback:

I received the boards...

And there's nothing wrong with them now! Getting S11 values of around -23dB and a loss of 1dB through the board.

Thanks for getting through all the headaches and getting this turned around.