



# Caliber Interconnect Solutions

Design for perfection

## SI & PI Simulation Case studies

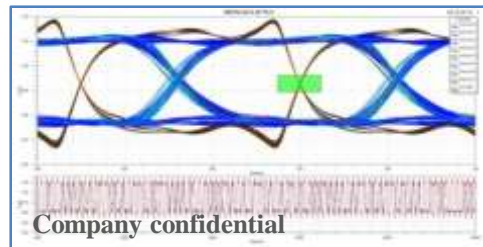
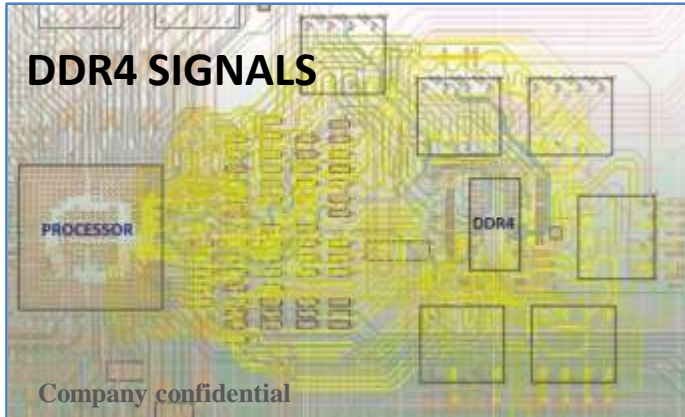


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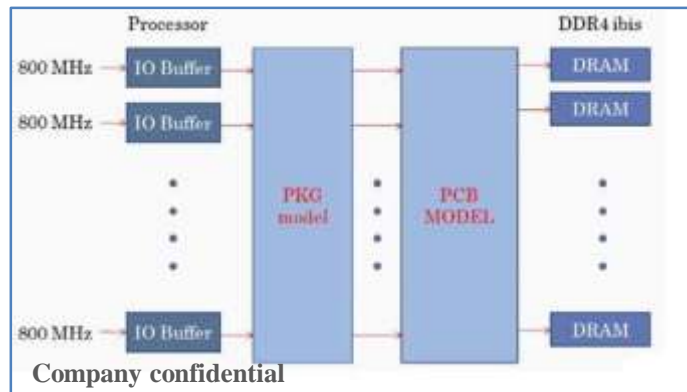
[www.caliberinterconnect.com](http://www.caliberinterconnect.com)



# EVALUATION BOARD WITH DDR4



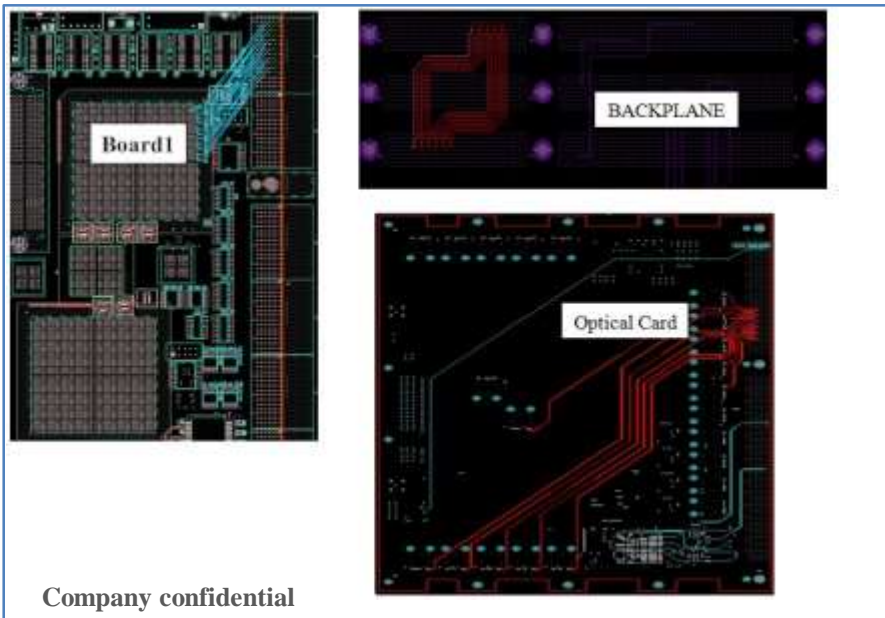
## BLOCK DIAGRAM



- 20 Layers Evaluation Board.
- Dielectric material : FR4 High Tg.
- 50Ohm for SE and 100Ohm for Differential signals.
- Datarate = 1600 Mbps
- Post Layout Simulation done for PKG+PCB.
- DDR4 Data signals simulated with different DSE and ODT condition.
- Eye mask is verified according to JEDEC DDR4 Standard.
- Ansys Siwave and Ansys Designer tool are used.

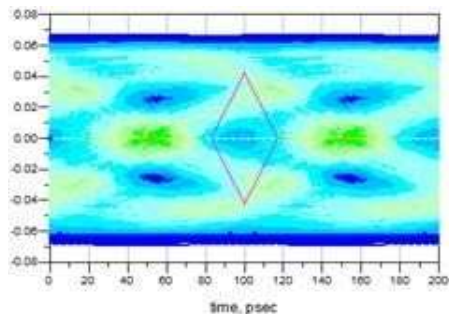


# 10G SERDES SIMULATION FOR APPLICATION BOARDS

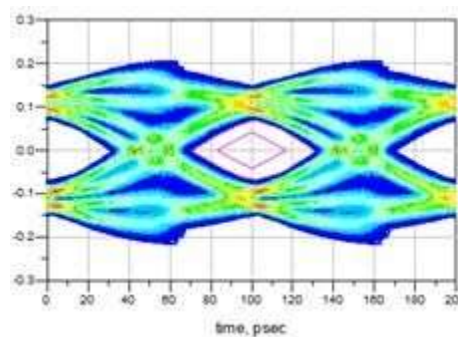


- SERDES Signals are connected from Board1 Processor to Optical PCB through backplane and connectors.
- Dielectric material : Nelco 4000-7 SI for all PCBs.
- Data rate = 10Gbps
- Post Layout Simulation is performed with with IBIS AMI model.
- Delivered AMIEqualization parameters to customer.
- Ansys Siwave and ADS tools are used.

**BEFORE AMI EQUALIZATION**



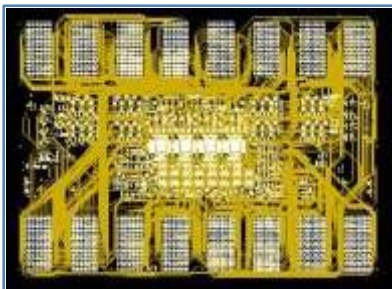
**AFTER AMI EQUALIZATION**



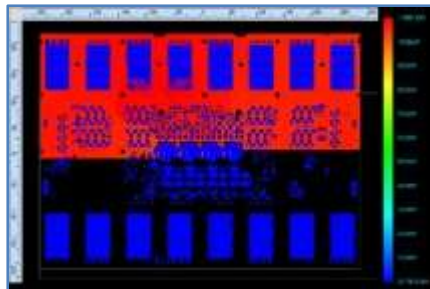


# 93k TEST BOARD POWER SIMULATION

93k Test Board Layoutview



Voltage distribution plot



DC ANALYSIS RESULTS BEFORE LAYOUT MODIFICATION

Node	Actual Voltage(V)	Voltage(V) referring to VRM	Current(A)	IR Drop Simulated	Specification	Pass/Fail
U1	1.010	1.010	54	0.00 = 0.000007(7%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Fail, F
U2	1.000	1.000	54	0.00 = 0.000000(0%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Fail, F
U3	1.000	1.000	54	0.00 = 0.000000(0%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Fail, F
U4	1.010	1.010	54	0.00 = 0.000007(7%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Fail, F

DC ANALYSIS RESULTS AFTER LAYOUT MODIFICATION

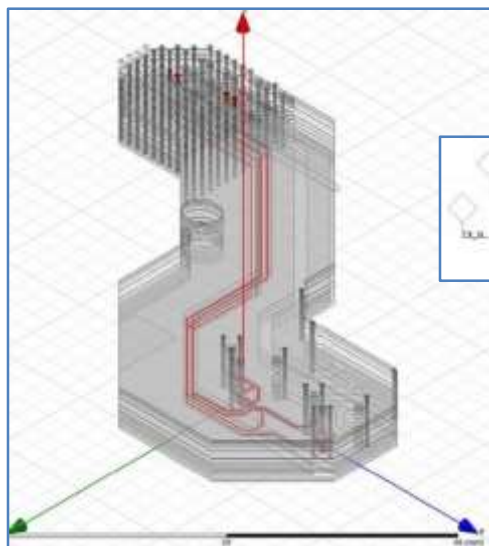
Node	Actual Voltage(V)	Voltage(V) referring to VRM	Current(A)	IR Drop Simulated	Specification	Pass/Fail
U1	1.077	1.077	54	0.00 = 0.000022(2%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Pass
U2	1.000	1.000	54	0.00 = 0.000000(0%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Pass
U3	1.000	1.000	54	0.00 = 0.000000(0%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Pass
U4	1.077	1.077	54	0.00 = 0.000022(2%) 0.00 = 0.000000(0%)	1.1 V, 5%, 1%	Pass

- 39 Layers 93k Test Board.
- Dielectric material : FR4 High Tg.
- Post Layout Voltage drop and Power impedance Simulation done for power nets in the layout.
- Layout is modified to achieve specification.
- Delivered Bulk and Decap Capacitors details.
- Cadence Sigrity Power DC is used for DC Analysis and OptimizePI is used for Capacitors optimization.



# 28Gbps LOOPBACK SIMULATION

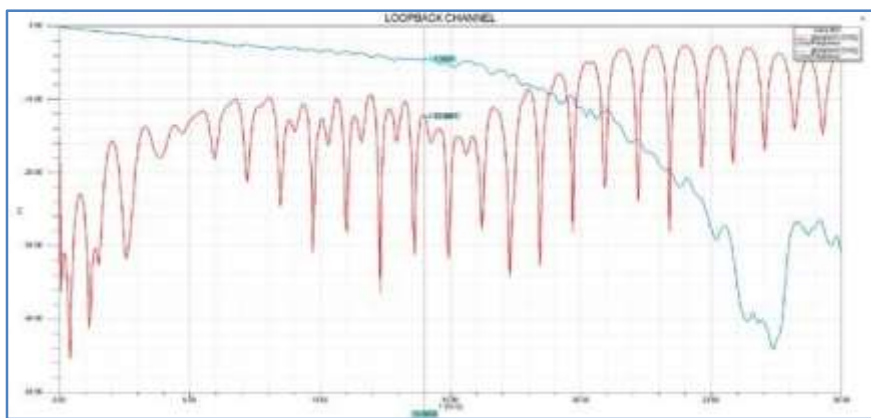
TX & RX Simulation in HFSS



Loop-back Topology



Insertion & Return Loss for 28G Loopback Channel



- 22 Layers board.
- Dielectric material: NELCO- 13SI
- 100Ohm controlled impedance for Differential pairs.
- Data rate =28Gbps
- Post Layout Simulation using 3D solver for more accurate result.
- Delivered optimized via structure for improved results.
- Ansys HFSS and Ansys Designer tools are used.



# Global Presence

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# Thank You

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